

SCHEDULE AT A GLANCE

Monday, September 14th 2009

Tutorials

Tuesday, September 15th 2009

Conference Opening

Technical Sessions

Welcome Reception

Wednesday, September 16th 2009

Technical Sessions

Conference Dinner

Thursday, September 17th 2009

Technical Sessions

Friday, September 18th 2009

Workshops

Sorin Cristoloveanu ENSERG-IMEP

Franz Dielacher Infineon

Christian Enz CSEM

Kazunari Ishimaru Toshiba

Hervé Mingam ST Microelectronics

Gaudenzio Meneghesso University of Padua

Ernesto Perea CEA/LETI

Hans-Jörg Pfeleiderer University of Ulm

Doris Schmitt-Landsiedel Technical University
of Munich

Hannu Tenhunen KTH Stockholm

Roland Thewes Qimonda

CONFERENCE VENUE

The 2009 ESSDERC-ESSCIRC Conference will be organized in Athens, Greece for the first time. Athens of today is a modern metropolis, a vibrant, appealing, hospitable and exciting city. Athens is also a cultural channel, the city of artists and a scientific centre. Athens, a gateway between the east and the west, hosts artistic happenings, festivals, conventions, athletic competitions, and celebrations.

Conference venue

The Divani Caravel Hotel faces the spectacular Acropolis and it is located few minutes walk from the city centre, and very close to the National Art Gallery, the Byzantine, the Cycladic Art and the Benaki museums, many major companies, shopping areas, embassies and historical sights.

KEY DATES

4th April 2009

Abstract submission deadline

22nd May 2009

Notification of acceptance

20th July 2009

Early registration deadline

ESSCIRC / ESSDERC STEERING COMMITTEE

Reinout Woltjer (Chair) NXP

William Redman-White (Co-Chair) NXP

Cor Claeys (Secretary) IMEC

Peter Ashburn University of
Southampton

Roberto Bez Numonyx

Ralf Brederlow Infineon

CONTACT INFORMATION

Local Organization

Institute of Microelectronics (IMEL)

NCSR 'Demokritos'

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Conference Secretariat

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ORGANISING COMMITTEE

Conference Chair Dimitris Tsoukalas,
NTU Athens

Deputy Chair Androula G. Nassiopoulou
IMEL/NCSR Demokritos

ESSDERC TPC Chairs

Chair Athanasios Dimoulas
NCSR Demokritos

Deputy Chair Pascal Normand
NCSR Demokritos

Vice Chair Francisco Gamiz
University of Granada

ESSCIRC TPC Chairs

Chair Yannis Papananos
NTU Athens

Deputy Chair Alexis Birbas
University of Patras

Vice Chair Angel Rodriguez-
Vazquez
University of Sevilla

Tutorials and Workshops Chairs

ESSCIRC: Matthias Bucher
Technical University of Crete

ESSDERC: Charalambos Dimitriadis
University of Thessaloniki

Fringe Poster Session Chairs

Panos Dimitrakis NCSR Demokritos
Stavros Chatzandroulis NCSR Demokritos

Local Organising Committee

Dimitris Tsamakias NTU Athens

Christos Tsamis NCSR Demokritos

Angela Arapoyanni University of Athens

Sotiria Galata NCSR Demokritos

Yerassimos Panayiotatos NCSR Demokritos

Harry Contopanagos NCSR Demokritos

Conference Secretariat

Efi Papastavropoulou Triaena Tours & Congress



<http://www.essderc2009.org>



<http://www.essderc2009.org>

ESSDERC

ATHENS-GREECE

14-18 September



DIVANI CARAVEL HOTEL

39th European Solid-State Device Research Conference

Paper submission deadline:

April 4th, 2009

Electronic submission

www.essderc2009.org



FINAL CALL FOR PAPERS

The aim of the ESSDERC conference is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and technologies. ESSDERC and its sister conference ESSCIRC, which deals with solid-state circuits, are governed by a single Steering Committee. The increasing level of integration for system-on-chip design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction among technologists, device experts, and circuit and system designers. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC will share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions. The main themes for original contributions to be submitted to ESSDERC 2009 include, but are not limited to the following:

Advanced CMOS devices

Ultimate CMOS scaling, high performance, low power and low voltage devices, novel MOS device architectures (double and multiple gate, vertical, ballistic), high-mobility channel engineered devices, SOI, SGOI, and SiON devices; SiGe, Ge, and strained devices.

Processing and Integration

Gate dielectrics, high k, gate stack, junction technology, cleaning and surface preparation, 3D integration and other novel processing schemes, interconnects, low k dielectrics, advances in integration for ULSI; SOI, SGOI; advanced/novel memory process integration; logic and mixed-mode IC manufacturing; RF integration (passives, active devices); photonics integration.

Telecommunication and power devices

RF CMOS, analog and mixed signal devices, passives, antennas, filters, RF MEMS, Bipolar, BiCMOS, compound semiconductors (GaAs, InP, GaN, SiC, alloys) and optoelectronic devices, integration of compound semiconductors with Si circuits, smart power devices, high-voltage, high power devices, high temperature operation, SiC devices, CMOS compatible power devices, IC cooling.

Modeling and Simulation

Numerical and analytical modeling of solid-state electronic and optoelectronic devices, quantum mechanical and non-stationary transport phenomena, ballistic transport, compact

circuit modeling for devices and interconnects, modeling and simulation of front-end and back-end fabrication processes, electro-thermal modeling and simulation.

Characterization and reliability

Characterization techniques, parameter extraction, advanced test structures and methodologies, reliability issues for new materials and devices (reliability of high-k and low-k materials), reliability of advanced interconnects, ESD, EMI, defect monitoring and control, metrology.

Memories

Embedded and stand-alone memories, DRAM, FeRAM, MRAM, PCRAM, CBRAM, Flash, SONOS, nanocrystal memories, single and few electron memories, 3D IC stacks, organic memories.

MEMS, Displays and SoC

Design, fabrication, modeling, reliability and packaging of all physical sensors and MEMS categories, bio-sensors for chemical, molecular and biological applications, BioMEMS, devices and technologies for lab-on-chip, integration of detectors, sensors, and actuators, CCDs and CMOS imagers, optical on chip communication, display technologies, TFTs, organic electronics, flexible substrate electronics, SoC and SiP packaging, microsystem packaging.

Emerging non-CMOS devices and technologies

Nanowires and nanoparticles for electronic, optoelectronic and sensor applications, carbon-based nanoelectronics and related nanodevices, materials and device related issues, single-electron, molecular and quantum devices, nanophotonics, spintronics, self-assembling methods, photonic devices.

ESSDERC/ESSCIRC JOINT SESSIONS

These sessions will focus on topics at the boundary between design and technology depending on the submitted abstracts. Contributions are solicited (but not limited) in the areas of circuit design and simulation techniques for process variability in nm-scale technologies as well as of microwave components over silicon substrates.

A panel discussion will be organized by **Dimitri Antoniadis** (MIT) on 'Technology, Circuit and System Co-Design in the New Scaling Era' with expert panelists from industry and academia.

JOINT PLENARY TALKS

Joachim Burghartz (IMS CHIPS)
'Ultra-thin Chips and Related Applications - A New Paradigm in Silicon Technology'

Tze-chiang (T.C.) Chen (IBM)
'Challenges for silicon technology scaling in Nanoscale Era'

Carlo Cognetti (STMicroelectronics)
'The impact of semiconductor packaging technologies on system integration: An Overview'

Michael Rookes (Caltech)
'Nano Electro-Mechanical devices: A new opportunity for microelectronics'

Tadashi Shibata (University of Tokyo)
'Bio-inspired devices and circuits'

Victor Zhirnov (SRC)
'Scaling beyond CMOS'

ESSDERC PLENARY TALKS

Joerg Appenzeller (Purdue University)
'Nanowire Electronics'

Sokrates Pantelides (Vanderbilt University)
'Performance, reliability, and aging of MOSFETs - From atomic-scale physics to engineering modeling'

Rainer Waser (RWTH-Aachen)
'Function by defects at the atomic scale - new concepts for non-volatile memories'

TUTORIALS AND WORKSHOPS

A Tutorial Day will be organized on Monday, September 14th, 2009, while a Workshop Day will take place on Friday, September 18th, 2009.

BEST PAPER AWARD

Papers presented at the conference will be considered for the Best Paper Award and for the best 'Young Scientist' Paper Award. The selection will be based on the results of the paper selection process and the judgment of the conference participants. The award delivery will take place at ESSDERC 2010.

PAPER SUBMISSION

The 2009 ESSDERC conference will allow only electronic submission of papers in PDF format. Prospective authors must submit their paper(s) via the conference website. Papers must be submitted in the final format to be published in the proceedings. They must not exceed four A4 pages with all illustrations and references included. The size of the PDF files submitted should not exceed 2 MBytes. Manuscript guidelines as well as instructions on how to submit electronically will be available on the conference website.

www.essderc2009.org

All paper submissions must be received by April 4th, 2009.

After selection of papers, the authors will be informed of the decision of the Technical Program Committee by e-mail at the beginning of June 2009. At the same time, the complete program will be published on the conference website.

The working language of the conference is English, which must also be used for all presentations and printed material.

REVIEW PROCESS

Papers submitted for review must clearly state:

- The purpose of the work
- How and to what extent it advances the state-of-the-art
- Specific results and their impact

The degree to which the paper deals with the above issues is fundamental to a successful review and selection of the paper. The most frequent cause of rejections of submitted papers is a lack of new results. Only work that has not been previously published at the time of the conference will be considered. Submission of a paper for review and subsequent acceptance is considered by the committee as a commitment

that the work will not be placed in the public domain prior to the conference.

Fringe Poster Session

Following a successful 'fringe' event during last Conference in Edinburgh, ESSCIRC and ESSDERC will be holding also a «fringe» event in addition to the main conference in Athens. The Fringe forum is ideally suited for the submissions of recent progress which may, in some cases, not be ready for a full paper submission. The emphasis of fringe submissions should be on the presentation of the latest data (both measurement and/or simulation) and new ideas. This forum provides the opportunity to network with the ESSDERC/CIRC community to discuss these ideas and latest results. Reviewing will be undertaken by a sub-committee under the main Technical Programme committee, and a separate proceedings will be published on CD for this event. To attract the latest results, submissions close at the later date of 12 June 2009. Submissions will be in the form of abstracts of one page of text and two pages of figures. Submission will be via the website www.esscirc2009.org/fringe, where further details can be found.