



Posters can be displayed from Tuesday (15/9) 9:00 till Thursday (17/9) 18:00. The Fringe-poster session being on Tuesday to Thursday during the coffee breaks in the free area in front of the conference rooms. Please refer to the timetable for further details. Presenters will also be on hand to discuss their posters outside this timeslot by prior arrangement.

- P1** Daniel Durini, Rana Mahdi, Andreas Spickermann, Werner Brockherde, Anton Grabmaier, Bedrich J. Hosticka,
"Lateral Drift-Field Photodetector Based on a Non-Uniform Lateral Doping Profile Photodiode for Time-Of-Flight Imaging"
- P2** Kai Sun, Mohammad M.A. Hakim, Peter Ashburn,
"Fluorine Dose Effect on the Nickel-induced Lateral Crystallization of Amorphous Silicon"
- P3** Sophie Puget, Germain Bossu, Pascal Masson, Pascale Mazoyer, Jean-Michel Portal, Philippe Lorenzini, Denis Rideau, Rachid Bouchakour, Thomas Skotnicki,
"Quantum Effect Modeling in Thin Film Independent Double Gate Capacitorless eDRAM"
- P4** S. Martinie, D. Munteanu, G. Le Carval, E. Sarrazin, S. Barraud, M-A. Jaud, J.L. Autran,
"Numerical simulation of ballistic/quasi-ballistic transport in FDSOI and Nanowire MOSFETs: analysis of CMOS inverter static performances"
- P5** Krzysztof Piskorski,
"Photoelectric methods of the flat-band voltage determination"
- P6** Davide Garetto, Erwan Dornel, Denis Rideau, William F. Clark, Alexandre Schmid, Saadia Hniki, Clement Tavernier, Hervé Jaouen, Yusuf Leblebici,
"Analytical and compact models of the ONO capacitance in embedded non-volatile flash devices"
- P7** Ji-Ting Liang and Chun-Hsing Shih,
"Multi-Level Schottky Barrier Charge-Trapping Non-Volatile Memory"
- P8** Guntrade Roll, Matthias Goldbach, Andre Wachowiak, Stefan Jakschik, Lothar Frey,
"Gate Edge Optimization for LSTP High-k Metal Gate Technology"
- P9** P. Baine, H. Gamble, B. Armstrong, S.J.N. Mitchell, D.W. McNeill, P. Rainey, Y.H.Low, Y.W. Low, D. Tantraviwat,
"Low Temperature Measurement of TFT,s Fabricated on Germanium-On-Sapphire Substrates"

- P10 Michaela Weidemann, Alexander Kloes, Mike Schwarz, Benjamin Iniguez, *"2D Physics-Based Compact Model of Channel Length Modulation for Asymmetrically Biased Double-Gate MOSFETs"*
- P11 Yiorgos Bontzios, Alkis Hatzopoulos, *"A Margarita Shaped Inductor Offering Wider Frequency Range in Comparison with Spiral Inductors"*
- P12 Mike Schwarz, Michaela Weidemann, Alexander Kloes, Benjamín Iñíguez, *"2D Analytical Solution of Potential in Lightly Doped Schottky Barrier Double-Gate MOSFET"*
- P13 Bing-Yue Tsui, Hsiao-Yu Chang, Chun-Kai Wang, Chi-Chung Kei, Chien-Nan Hsiao, *"Carbon Nanotubes as Charge Storage Nodes for Non-volatile Memories"*
- P14 Edmundo A. Gutierrez-D., A. Torres-J., J. de la Hidalga-W, I. Juarez-R., *"Room-temperature quantum-wire-like conduction stimulated by magnetic field in a high-index (5 5 12) nMOS structure"*
- P15 L. Nougaret, G. Dambrine, S. Lepilliet, H. Happy, N.Chimot, V. Derycke, J. - P. Bourgoin, *"Looking behind the mirror: GHz characterization of high impedance 1D nano-objects"*
- P16 Leonidas Tsetseris and Sokrates T. Pantelides, *"Morphology and defect properties of Ge-GeO interfaces"*
- P17 Choudhury Jayant Praharaj, *"Effect of Polarization on Base Resistance and Frequency Response of GaN/InGaN Heterojunction Bipolar Transistors"*
- P18 V. Constantoudis, G.P. Patsis, E. Gogolides, *"The role of gate width in transistor performance: Effects of gate sidewall roughness"*
- P19 Evangelos A. Angelopoulos, Michael Wiesner, Saleh Ferwana, Joachim N. Burghartz, *"Compliant Substrate based on Sintered Porous Silicon for the Local Integration of Heterodevices with Silicon Microelectronics"*
- P20 V. Tsouti, C. Boutopoulos, P. Andreakou, M. Ioannou, I. Zergioti, D. Goustouridis, S. Chatzandroulis, J. Hue, R. Rousier, D. Kafetzopoulos, D. Tsoukalas, P. Normand, *"Capacitive DNA Sensing Using Ultrathin Si Membranes"*
- P21 M.Mongillo, G.Katsaros, P.Spathis, P.Gentile, C.Mouchet, E.Rouviere, S. de Franceschi, *"Silicon nanowires: functionality at the nanoscale"*
- P22 P.E. Coulon, B. S. Sahu, M. Carrada, S. Schamm, G. Ben Assayag, B. Pecassou, A. Slaoui, S. Lhostis, C. Bonafos, *"Ultra-Low Energy Ion Implantation of Si and Ge into HfO₂-based layers for Non Volatile Memory Applications"*

- P23 F. Zacharatos, H. Contopanagos, A. G. Nassiopoulou,
"Porous Si microplate technology as a low RF-loss substrate for on-chip RF isolation"
- P24 P. E. Coulon, L. Lamagna, C. Wiemer, S. Baldovino, A. Molle, M. Perego,
M. Fanciulli, S. Schamm,
*"Dielectric Constant Analysis of High-k/Si(Ge) Stacks Based on
Transmission Electron Microscopy and Electrical Characterization"*
- P25 Shin-Nyoung Kim, Dong-Ho Choi, Jae-Woo Park, Changsik Yoo,
*"A 1.8-29.2MHz Analog Channel Selection Filter with Automatic Frequency
Tuning for Reconfigurable RF Transceiver in 0.18 μm CMOS"*
- P26 Felix Lang, Thomas Alpert, Damir Ferenci, Markus Grözing, Manfred
Berroth,
"Design of a 25 GS/s 6-bit Flash-ADC in 90 nm CMOS technology"
- P27 Thomas Alpert, Felix Lang, Markus Grözing, Manfred Berroth,
"25 GS/s 6-bit Pseudo Segmented Current Steering DAC in 90 nm CMOS"
- P28 Mathieu Moreau, Daniela Munteanu, Jean-Luc Autran,
*"Quantum Simulation Analysis of Gate Tunneling Current in High-k Gate
Stack MIM Capacitors"*
- P29 Nasir Uddin and Andreas Thiede,
"Integrated Active Sensors for Near-Field Measurement"
- P30 Yu Ben, Laurent El Ghaoui, Kameshwar Poolla, Costas J. Spanos,
"Chance-constrained Digital Circuit Sizing"
- P31 Yuji Osaki, Tetsuya Hirose, Kei Matsumoto, Nobutaka Kuroki, Masahiro
Numa,
"Variation Tolerant Subthreshold Adder Design for Ultra-low Power LSIs"
- P32 Marcus Weis, Philip Teichmann, Tamara Seybold, Dominik Kasprovicz,
Andrzej Pfitzner, Wojciech Maly, Doris Schmitt-Landsiedel,
"Adiabatic Circuits using Vertical Slit Field Effect Transistor"
- P33 Philipp Kruppa, Alexander Frey, Meinrad Schienle, Ingo Kühne, Doris
Schmidt-Landsiedel,
"Digital CMOS-based Chronocoulometric DNA-Sensor Array Platform"
- P34 Florian R. Chouard, Michael Fulde, Doris Schmitt-Landsiedel,
"Impact of Degradation Mechanisms on Analog Differential Amplifiers"
- P35 Thomas Veigel, Markus Grözing, Manfred Berroth, Fred Buchali,
"Design of a Viterbi Equalizer Circuit for Data Rates up to 43 Gb/s"
- P36 Min-su Kim, Jae-Hyuk Oh, Chil-Gee Lee, Bai-Sun Kong,
"Dynamic Differential Flip-Flop without Explicit Output Latching Stage"
- P37 Djordje Marinkovic, Alexander Frey, Ingo Kühne, Gerd Scholl,
"A new power processing circuit for an energy-harvesting wireless node"

- P38 Ramy Iskander, Marie-Minerve Louërat, Andreas Kaiser,
“Design and Analysis of Analog Firm IPs using Hierarchical Sizing and Biasing Methodology”
- P39 G. Raikos and S. Vlassis,
“Low-Voltage Differential Voltage Follower”
- P40 Eleni-Sotiria A. Kytonaki and Yannis Papananos,
“Multi-band, Differentially Tuned Current Adjusted, Voltage Controlled Oscillator with Quadrature Outputs”
- P41 Shubha Bommalingaihanapallya and Ramesh Harjani,
“Multi-Rate Sigma-Delta Converter”
- P42 Panagiotis Broutas, Stathis Kyriakis Bitzaros, Ioannis Mourtsiadis, Dimitrios Goustouridis, Stavros Katsafouros, Dimitrios Tsoukalas, Stavros Chatzandroulis,
“Power Harvesting Scheme for Remotely Powered Sensor Tags”