ESSCIRC 2009, September 14, half-day (9-12) Tutorial on

Nanoscale CMOS Analog Design from Devices to System

Organizer: Matthias Bucher, Technical University of Crete (TUC), Chania, GREECE

Presenters: Matthias Bucher, TUC, Chania, Greece
Maher Kayal, EPFL, Lausanne, Switzerland
Georges Gielen, KUL, Leuven, Belgium

Abstract: The increasing complexity of nanoscale CMOS technology imposes important constraints on the design of analog integrated circuits: while circuit performance using downscaled CMOS is largely improved in terms of speed, while other analog figures of merit, such as transistor gain, are degraded. Reduced voltage headroom often requires the adoption of ultra-low-voltage techniques particularly in moderate inversion. Furthermore, variability is an important bottleneck impairing design in scaled technologies. The tutorial covers issues ranging from technology and compact modelling aspects, to analog circuit design retargeting and methodologies for variability reduction using digital tuning, and optimization aspects on the system level.

1 Program

9:00 – 9:50	**CMOS Device Modeling for Analog/RF Design** *M. Bucher* *TUC, Chania, Greece*
9:50 – 10:40	**Transistor Level Analog Design in Nanoscale CMOS** *M. Kayal* *EPFL, Switzerland*
10:40 – 11:10	Break
11:10 – 12:00	**System Level Design and Verification in Nanoscale CMOS** *G. Gielen* *KUL, Belgium*
12:00 – 13:30	Lunch Break

2 Abstracts and Bios

CMOS Device Modeling for Analog/RF Design

***M. Bucher**, TUC, Greece*

Abstract: The design of low-voltage, low-power and RF CMOS integrated circuits benefits largely from operation in moderate inversion. Often, best overall circuit trade-offs among power consumption, gain, linearity, matching and noise is achieved in moderate inversion, including for circuits operating at high frequencies. This trend is reinforced in advanced CMOS technology due to lower supply voltages. However, traditional design methods in this important region fail, while characterization methods rarely address this important region. The lecture will discuss a charge modelling approach, based on the EKV MOS transistor model, covering DC to high-frequency operation, characterization, noise and mismatch. Scaling trends for advanced CMOS technology are examined in view of analog properties. Finally, the advanced EKV3 MOSFET compact model for analog/RF IC design is reviewed.

Matthias Bucher received his MSc. and Ph.D. degrees in Electrical Engineering from the Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland in 1993 and 1999 respectively. In 1997, he was a visiting researcher at LSI Logic, Milpitas, California. From 2000 to 2003, he was a postdoctoral researcher at National Technical University of Athens, Greece, as well as a consultant for microelectronics industry. Since 2004, Matthias Bucher is an Assistant Professor at the Department of Electronic and Computer Engineering, Technical University of Crete (TUC), Chania, Greece, where he currently is the Director of the Electronics Laboratory. His research interests are in the design of low-power, analog and RF integrated circuits (ICs), in the characterization and compact modelling of nanoscale devices, as well as in the development of CAD tools. Matthias Bucher has coordinated the development of the EKV3 MOSFET advanced compact model for circuit simulation. He has authored or co-authored over 50 papers in international journals and conferences. He is a member of the Technical Program Committee of IEEE DDECS and serves as Chairman for Tutorials and Workshops of the European Solid-State Circuits Conference (ESSCIRC), Athens, Greece, 2009.

Transistor Level Analog Design in Nanoscale CMOS

***M. Kayal**, EPFL, Switzerland*

Abstract: Many analog circuit topologies, which have served the design community well for many years, cannot be used in very deep submicron technology. The lecture is dedicated to review the techniques of implementation that make analog circuits possible and will depict the limitation of the retargeting aspect.
The proposed topics will start from the basic analog structures (gain cells, biasing, references) going toward the operational transconductance amplifiers, OpAmp, comparator topologies including robust biasing techniques. A mixed-mode approach using digital algorithms will be presented to improve some degradation aspects inherent to technology evolution such as variability. Structure of the lecture: 1) Analog circuits design challenges and opportunities; 2) Inversion factor based design methodology for: Basic analog structures, OTA topologies, OpAMP topologies; 3) Variability enhancement using digital tuning approaches.

Maher Kayal received the M.S. and Ph.D degrees in electrical engineering from the Ecole Polytechnique Fédérale de Lausanne (EPFL, Switzerland) in 1983 and 1989 respectively. He has been with the Electronics laboratories of the Ecole Polytechnique Fédérale de Lausanne (EPFL, Switzerland) since 1990, where he is currently a professor, head of the electrical and electronics section and vice dean for education of the school of engineering. He has published many scientific papers, has co-authored three text books dedicated to mixed-mode CMOS design, and holds five patents. His technical contributions are in the area of analog and Mixed-signal circuits design including highly linear and tunable sensor microsystems, signal processing and CAD tools for Analog design and layout automation.

System Level Design and Verification in Nanoscale CMOS

***G. Gielen**, KUL, Belgium*

Abstract: Tbd.

Bio: Tbd.