**Title of Tutorial: Disruptive Technologies for More Moore**

* **JP Colinge** (10 min + 5 min questions) Tyndall – Ireland

*Introduction: Issues with device scaling and emerging device options*

* **S. Deleonibus** (50 min + 10 min questions) CEA LETI –France

*Electronic Devices Architectures for the NANO-CMOS Era. From Ultimate CMOS Scaling to Beyond CMOS devices*

* **A. Ionescu** (50 min + 10 min questions) EPFL - Switzerland

*Sub kT/q subthreshold slope transistors*

* **S. Okhonin** (50 min + 10 min questions) Innovative Silicon - Switzerland

*ZRAM (Limits of DRAM)*

* **T. Kawahara** (50 min + 10 min questions) Hitachi – Japan

*Spin-Transfer Torque RAM: A low-power Flash Memory substitute*

## SHORT BIOS AND ABSTACTS OF THE PRESENTATIONS

**Prof. Jean-Pierre Colinge** received a BS degree in Philosophy, the Electrical Engineer degree, and the Ph.D. degree in Applied Sciences from the Université catholique de Louvain, Louvain-la-Neuve, Belgium, in 1980, 1980, and 1984, respectively. He worked at the Centre National d'Etudes des Télécommunications (CNET), Meylan, France, at the Hewlett-Packard Laboratories, Palo Alto, USA, at IMEC, Leuven, Belgium, where he was involved in SOI technology for VLSI and special device applications. From 1991 to 1997, Dr. Colinge was professor at the Université catholique de Louvain, leading a research team in the field of SOI technology for low-power, radiation-hard, high-temperature and RF applications as well as reduced-dimension devices (thin double-gate and quantum-wire MOSFETs). He has published over 315 scientific papers and four books on the field of SOI as well as two books on semiconductor device physics. Prof. Colinge is currently Professor at the Tyndall National Institute, University College Cork, Ireland, where he is head of the Micro-Nano Electronics Centre and is conducting research on the modeling, fabrication and characterization of advanced SOI MOS devices.

**SIMON DELEONIBUS** received the MSc in Physics and PhD degrees in Applied Physics from Paris University in 1979 and 1982 respectively. He joined Thomson Semiconducteurs (Grenoble) in 1981. He joined LETI(CEA) in 1986 as expert on CMOS and Flash memories integration. From 1996 to 2008, he directed the Electronic Nanodevices Laboratory(60 researchers), leading several industrial, National and European projects. He is now Chief Scientist of LETI-Silicon Technologies (850 researchers).
Published more than 500 papers (conferences and journals ; 50 invited) and owns 30 patents; Editor of 1 book (WSPC). Author of 8 book chapters.
Editor of IEEE Transactions on Electron Devices.
Member of Conferences Program Committees such as IEDM, VLSI Tech Symposium, ESSDERC, ECS Symposia, ITRS. Member of Board of Directors of Nanosciences Foundation and Panelist European Research Council.
IEEE Fellow ; French CEA Research Director; IEEE Distinguished Lecturer; "Chevalier de l'Ordre National du Mérite" by French Presidence Decree; Recipient of the "2005 Grand Prix de l'Académie des Technologies". Co-recipient of 7 Best Papers Awards.

**Abstract of Short Course**

The microelectronics industry is facing historical challenges to down scale CMOS devices through the demand for low voltage, low power, high performance and increased functionalities. The implementation of new materials and devices architectures will be necessary. The introduction of HiK/metal gate stack is among the most strategic options to reduce power consumption and manage low supply voltage. Multigate , multichannels, sub 60mV/dec swing architectures based on wrapped around nanowires increase MOSFETs drivability, will reduce power at the Lg=5nm level, and allow new memory devices opportunities. By introducing new materials(HiK, Ge, III-V, Carbon based materials like diamond, graphene and CNTs, molecules,…), and new functions such as sensing and actuation allowing to interface the outside world, Si based CMOS will be scaled beyond the ITRS as the System-on-Chip/Wafer Platform[3] (Fig. 2). The Heterogeneous integration of these devices with CMOS will require new 3D and Packaging schemes leading to the increase of effective packing density, functionalities and improving systems figures of merit.

**Adrian M. Ionescu** is an Associate Professor at the Swiss Federal Institute of Technology Lausanne (EPFL), Switzerland. He is currently the Head of the Nanoelectronic Devices Laboratory (Nanolab) and Director of the Doctoral School of Microsystems and Microelectronics of EPFL. Prof. Ionescu has published more than 200 articles in international journals and conference proceedings. He served on the International Electron Devices Meeting conference technical committees in 2003/2004 and 2008/2009. He was the Technical Program Committee Chair of the European Solid-State Device Research Conference in 2006. He is a member of the Scientific Committee of the Cluster for Application and Technology Research in Europe on Nanoelectronics

(CATRENE) and was appointed as the national academic representative of Switzerland to the European Nanoelectronics Initiative Advisory Council (ENIAC).

## Abstract of short course

Power dissipation in switching devices is considered as an important roadblock for future nanoelectronic circuits and systems. The power aware (energy efficient) devices define an exciting research domain for physics, technology and novel device architectures. In this tutorial we will present energy efficient device architectures that can provide a much steeper transition than the 60mV/decade limit of MOSFET at room temperature, with particular focus on: (i) tunnel FETs and (ii) emerging positive-feedback gate FET. Some of their key properties and their potential for low power logic and memory circuits as well as for power management will be discussed.

**Serguei Okhonin** received his M. Sc. in Physics from Novosibirsk State University and his PhD degree from Swiss Federal Institute of Technology (EPFL). From 1980 to 1993 he worked as Research Associate at the Institute of Semiconductor Physics, Novosibirsk, Russia, focusing on semiconductor device physics. From 1994 to 2003 he worked as Research Associate at IMO and LEG, EPFL. He took part in several European projects focused on advanced CMOS technology development.

In 2002 he co-founded Innovative Silicon, an IP company developing a new SOI single transistor memory technology. He acted as CTO and he is currently Chief Scientist at Innovative Silicon. He has authored or co-authored more than 50 papers and filed more than 40 patents

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**Awards:**
EETimes ACE Awards "Innovator of the Year" 2007 - Finalist
http://www.innovativesilicon.com/en/pdf/ACE_finalist_PR_final3.pdf
IEEE Spectrum ACE Award for Emerging Technology 2007
http://www.innovativesilicon.com/en/pdf/IEEE_Award_Final1.pdf

## Abstract of short Course

In1966, Dr. Robert H. Dennard, a Fellow at the IBM created the one-transistor DRAM (Dynamic Random Access Memory). In 1970 Intel released the first DRAM chip, a 1K PMOS device. Since that time, the basic DRAM building block has consisted of a single transistor and an increasingly complex capacitor.

The DRAM industry has achieved miracles cramming more and more memory bits onto ever smaller silicon die – and selling it for cents. Process engineers have performed heroically, especially with respect to the capacitor element, which has become harder and harder to scale – a problem which is exacerbated as device geometries shrink.

We are fast-approaching the scaling limits for the capacitor element, and it is clearly time for a new approach. The DRAM industry – including producers and consumers – needs a better DRAM. There appears to be a ground swell of opinion in the commercial world and the analyst community that Floating Body memories may provide the answer.

**Takayuki Kawahara** received B.S. and M.S. degrees in physics in 1983 and 1985, and Ph.D. degree in electronics in 1993 from Kyushu University, Fukuoka, Japan. In 1985, he joined Central Research Laboratory, Hitachi Ltd. Since then, he has made many contributions in the field of low-voltage low-power memories. That includes the gate-source self-reverse biasing circuit to reduce subthreshold current, charge-recycling scheme, and the back-gate-controlled thin BOX FD-SOI technology. Currently, his mission is exploring a new concept memory, especially focused on spin-transfer torque memory.

He was a visiting researcher at Electronics Laboratory (LEG), Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland from 1997 to 1998. He has been a member of the ISSCC program committee since 2000, and now serves as the FE regional chair. He is a fellow of IEEE and an IEEE SSCS Distinguished Lecturer.

## Abstract of short Course

Spintronics is the technology that brings us the new features and values by controlling spin (magnetization) with electronics. That will break the cooped-up current technology. Among them, SPin-transfer torque RAM (SPRAM) is the most influential device, which leads the innovation in computing architecture and equipment configuration by enabling normally-off and instantly-on functions. SRAM and DRAM have an infinite number of write cycle but these are volatile. Flash memory is a nonvolatile but has limited number of write cycle. SPRAM, on the contrary, has nonvolatility and infinite write cycle at the same time. This memory is the most promising candidate of universal memory, the breaker of Moore. In this talk, after reviewing the general spintronics and its applications, the principles and operation of SPRAM is described in detail with an example of our current 32Mb chip. And show you that this memory will enable us to live in the rich but sustainable green IT world in near future.